GMX™ DMA SASI INTERFACE BOARD

User's Manual

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GIMIX DMA SASI INTERFACE BOARD

FEATURES

* Interfaces up to five intelligent peripheral controllers to the SS-50/C bus.
* Uses High-speed Direct Memory Access (cycle steal) and/or programmed I/O data transfers to and from the host system.
* Automatically generates handshake signals for the SASI bus.
* Guaranteed operation in 2 MHz. systems.

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INTRODUCTION

The GIMIX DMA SASI INTERFACE BOARD provides a means of interfacing the SS-50 bus with peripherals that use the Shugart Associates System Interface (SASI). SASI is an interface standard designed to connect computer systems to intelligent mass-storage controllers.

The GIMIX DMA SASI INTERFACE supports the SASI standard, with the exception of Parity, and will handle a maximum of five (5) separate controllers. The host system communicates with the controller over an 8-bit data bus and 8 separate control lines for handshaking. The board supports high-speed DMA as well as programmed I/O data transfer between the host system and the controller. A command/status register allows the host to control board functions and monitor the status of the interface.

This manual describes the basic hardware features and operation of the board. Since the interface can be used with a variety of different controllers, no information on specific implementations is included in this manual. For more information see the documentation for the controller being used.

SECTION 1: HARDWARE CONFIGURATION

1-1: Addressing

The GIMIX DMA SASI INTERFACE BOARD occupies 8 bytes of address space and may be located on any 8 byte boundary in the address space. The base address for the board is selected by setting the appropriate sections of DIP-switches S1 and S2. The layout of these switches is shown in figure 1.

There are 17 switch sections, labeled A3 through A19, that correspond to the 17 high-order system address lines. These switches must be set to correspond to the bit pattern of the desired address. A switch section that is OFF (OPEN) corresponds to a zero (0) and a switch section that is ON (CLOSED) a one (1).

A separate switch (S2, section 10) enables and disables the decoding of the upper 4 address lines (A16-A19) for extended addressing. In systems that require that the I/O devices be fully decoded (OS-9 GMX III, and OS-9 GMX II with the CPU modified for 64K pages) this switch must be ON (CLOSED) and the appropriate extended address must be selected on A16-A19. In system that do not use extended addressing (FLEX-only and FLEX/OS-9 GMX I systems), and systems that do not require fully decoded I/O (OS-9 GMX II with an unmodified CPU), S2-10 should be OFF (OPEN) to disable extended address decoding.

Figure 1 shows the standard addressing for the board when used with GIMIX versions of FLEX and OS-9. The example shows S2-10 ON for fully decoded I/O (OS-9 GMX III and GMX II w/modified CPU). For systems that do not require extended address decoding S2-10 should be OFF (FLEX, FLEX/OS-9 GMX I, OS-9 GMX II w/unmodified CPU).

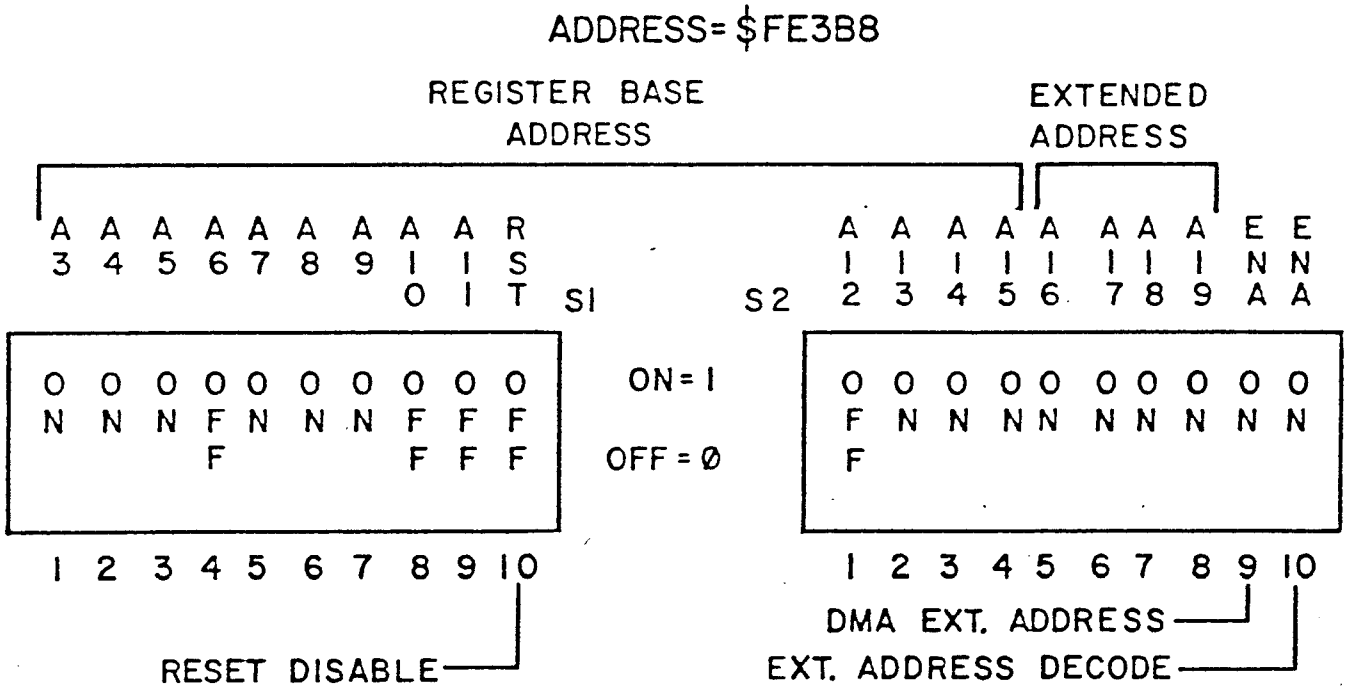


Figure 1

1-2: Extended Address Output

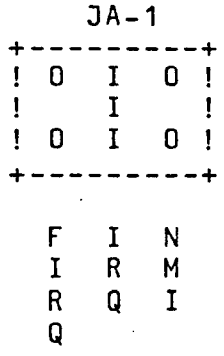
Since the board uses DMA (Direct Memory Access), it is capable of driving the system address bus. A separate switch (S2-9) enables or disables the address output from the board to the four extended address lines (A16-A19). This switch must be ON (CLOSED) for systems that use extended addressing (OS-9 GMX II and III, and UniFLEX) and OFF (OPEN) for systems that do not use extended addressing (FLEX and OS-9 GMX I). NOTE: Although FLEX systems running VDISK use the extended addressing, S2-9 does not need to be ON unless the system is setup for software switching with OS-9 GMX II or III.

1-3: Reset Option

The SASI reset signal (RST), used to reset the external controller, may be asserted by setting the appropriate bit in the board control register (see the control register section) and, optionally, whenever a system (bus) reset occurs. This option is controlled by DIP-switch S1, section 10. When S1-10 is ON (CLOSED), RST may only be asserted by writing to the control register. When S1-10 is OFF (OPEN), RST is also asserted anytime a system (bus) reset occurs. Normally this switch should be in the OFF position (reset enabled).

1-4: Interrupt Option Jumper (JA-1)

Jumper area JA-1 selects the type of interrupt generated by the interface when interrupts are used. This jumper is factory configured for IRQ interrupts. Should NMI or FIRQ interrupts be required for a special application a trace must be cut and the appropriate jumper installed. The interrupt output is enabled by a bit in the control/status register.



SECTION 2: BOARD REGISTERS

Of the 8 bytes occupied by the board, only the first five (0-4) are used; bytes 5 through 7 are a repeat of the fourth byte. The following table shows the address assignments:

ADDRESS	FUNCTION	
[x]xxx0	Control/Status register	(read/write)
[x]xxx1	DMA address register (A19-A16)	(write only)
[x]xxx2	DMA address register (A15-A8)	(write only)
[x]xxx3	DMA address register (A7-A0)	(write only)
[x]xxx4	SASI data port	(read/write)
[x]xxx5	" " " repeats	
[x]xxx6	" " " repeats	
[x]xxx7	" " " repeats	

[x] = extended address if used

2-1: Control/Status Register ([x]xxx0)

Reads of this register return status information from the SASI bus and the interface board. Writes are used to select one of the five controllers that the board can access and to program certain interface functions. The following tables show the bit map of the control/status register.

Control/Status Register (read)

	BIT	NAME	SOURCE	FUNCTION
LSB	Bit 0	REQ	SASI bus	1=request for data transfer to/from external controller
	Bit 1	MSG	SASI bus	1=second byte of command status is waiting to be read
	Bit 2	C/D	SASI bus	1=command block being sent or command status being received 0=data being sent or received
	Bit 3	BUSY	SASI bus	1=external controller busy 0=not busy
	Bit 4	I/O	SASI bus	1=data from SASI to host 0=data to SASI from host
	Bit 5	DMAE	interface	1=DMA transfer enabled 0=DMA transfer disabled
	Bit 6	INTE	interface	1=Interrupts to host enabled 0=Interrupts not enabled
MSB	Bit 7	INT	interface	1 only if (I/O=1 & C/D=1 & REQ=1) (command complete)

NOTE: The SASI handshake lines (B0-B4) are inverted between the SASI bus and this register. When a SASI handshake line is low (0) the associated bit in the status register is high (1).

Bits 0-4 are the inverse of the SASI bus control lines and are used to control the flow of data between the host and the controller(s). For more information on the function of these signals see the documentation for the controller being used. Note: The interface automatically performs the appropriate handshaking with the controller (using ACK and SEL) as data is read or written by the host.

Bit 5 enables/disables DMA data transfers between the SASI bus and the host. See the description of DMA operation for more information.

Bit 6 enables/disables interrupts from the interface to the host.

Bit 7 is the logical AND of bits 0, 2, and 4 (REQ, C/D, and I/O). When all three of these signals are high (1) (indicating completion of the current command) bit 7 is a 1, and if interrupts to the host are enabled [see bit 6 (write)], the host is interrupted. This bit is normally used by the host system to determine if the board is the source of an interrupt.

Control/Status Register (write)

	BIT	NAME	FUNCTION
LSB	B0-4	SEL0-4	Used to select one of the five controllers that may be connected to the interface.
	B5	DMAE	1 enables DMA transfers 0 disables DMA transfers
	B6	INTE	1 enables interrupts to host 0 disables interrupts to host
MSB	B7	RST	1 Asserts SASI RST line 0 Deasserts SASI RST line

Bits 0 through 4 are used to select one of five controllers that can be connected to the interface. One and only one of these bits must be set (1) to select a particular controller. When multiple controllers are used, each must be set to respond to a unique address. The standard, single controller configuration uses address 0 (zero) for the controller; bit 0 must be set (1) to select this controller.

Bit 5 is used to enable DMA data transfer between the interface and the host. When this bit is set (1), a DMA transfer will be initiated each time the controller requests a data-type transfer to the host. See the section on DMA operation for more information. When clear (0), no DMA will take place.

Bit 6 is used to enable or disable interrupt output from the interface to the host. When this bit is set (1), the host will be interrupted under the conditions described in the section on interrupts. When this bit is clear (0), no interrupts to the host are generated. Note: The type of interrupt generated is determined by jumper area JA-1 (normally IRQ).

Bit 7 allows the controller to be reset without generating a system reset. When this bit is set (1) the SASI reset line (RST) is asserted and remains so until the bit is cleared (0).

2-2: DMA Address Registers

The three DMA address registers are used to program the starting address for DMA data transfers between the controller and the host. If DMA transfer is enabled (DMAE bit set) these registers must be programmed to the required starting address before a command is issued to the controller that causes a data-type transfer. See the section on DMA operation for more information. The address is automatically incremented each time a byte is transferred.

The lower 4 bits of the register at [x]xxx1 set the beginning extended address (if required) as follows: B3=A19, B2=A18, B1=A17, and B0=A16. The upper 4 bits of this register are unused.

The register at [x]xxx2 sets the most significant 8 bits of the beginning address. (B7=A15, B6=A14, ..., B0=A8)

The register at [x]xxx3 sets the least significant 8 bits of the beginning address. (B7=A7, B6=A6, ..., B0=A0)

2-3: SASI Data Port [x]xxx4

This address is the 8-bit, bi-directional data port used to pass information between the host and the controller. The direction of the data flow is determined by the controller and indicated by the state of the I/O line. For example, when the controller is waiting for a command (as indicated by the state of the handshake lines) the host writes the command byte(s) to this address. When the state of the handshake lines indicates that the controller has status information ready, the host reads from this address.

SECTION 3: DMA OPERATION

There are basically two types of transfer that take place between the host and the controller, via the SASI interface. Commands/status transfers and data transfers. The host always issues commands to the controller and receives status information by monitoring the SASI handshake lines and writing or reading the data port ([x]xxx4). Data transfers can take place using the same method or, faster and more efficiently, by using high-speed DMA (Direct Memory Access).

Once the starting address for the DMA has been programmed in the DMA address registers and the DMA is enabled, DMA data transfers are automatic. When the controller, as the result of a command issued by the host, requests a data-type transfer (as indicated by the state of the C/D and MSG lines) the DMA circuitry is enabled and each subsequent assertion of the REQ line by the controller will cause a byte to be transferred. Each time a byte is transferred, the address register is incremented. This continues until the controller no longer requests a data-type transfer. The number of bytes transferred and the direction of the transfer are determined by the controller.

At the completion of a DMA transfer, the DMA address registers contain the memory address of the byte following the last byte transferred. The DMA address registers do not need to be reprogrammed if this address is correct for the next transfer that will be made.

The DMA uses a full 20-bit address counter and transfers can span any address range within the address space.

SECTION 4: INTERRUPTS

The interface can be programmed to interrupt the host when the controller has completed a command and is ready to output status information. The interrupt output can be enabled by setting Bit 6 of the control/status register ([x]xxx0) to a one (1).

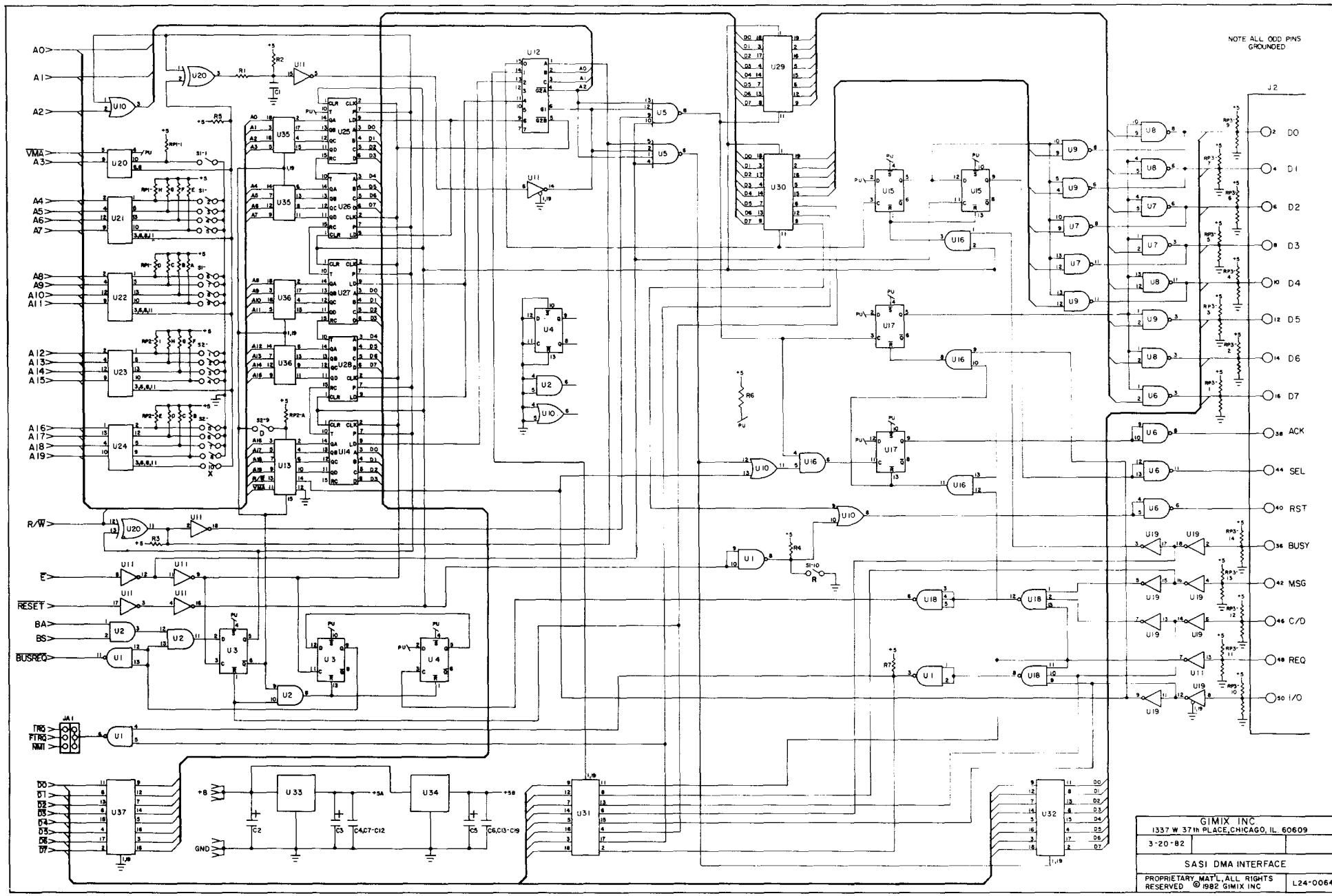
At the completion of a command (as indicated by the state of the I/O, C/D, and REQ lines) an interrupt is generated, if bit 6 is set, and Bit 7 (IRQ) of the control/status register will be set (1). This bit can be polled by the host when checking for the source of the interrupt. It is cleared automatically when the status bytes are read from the controller. Note: Bit 7 of the control/status register is not affected by the Interrupt Enable Bit (B6). It can be read at any time to determine if a command has been completed; even if the interrupt output is disabled (B6=0).

SECTION 5: EXTERNAL CONNECTIONS

Connection to the external controller is made through the 50 pin header connector (P2) located in the upper right corner of the board. The pinout of this connector matches the SASI standard and a 50-pin ribbon cable is used to interconnect the interface and controller.

The cable must be installed so that pin 1 on the interface board, located at the upper right corner of the connector, connects to pin 1 on the controller.

If multiple controllers are connected to a single board, the termination resistors must be removed from all but the last controller in the daisy-chain.


NOTE ALL ODD PINS GROUNDED
J2
2 D0
4 D1
6 D2
8 D3
10 D4
12 D5
14 D6
16 D7
38 ACK
44 SEL
40 RST
36 BUSY
42 MSG
46 C/D
48 REQ
50 I/O
A0
A1
A2
VMA
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
R/W
E
RESET
BA
BS
BUSREQ
IRQ
FIRQ
NMI
D0
D1
D2
D3
D4
D5
D6
D7
+8
GND
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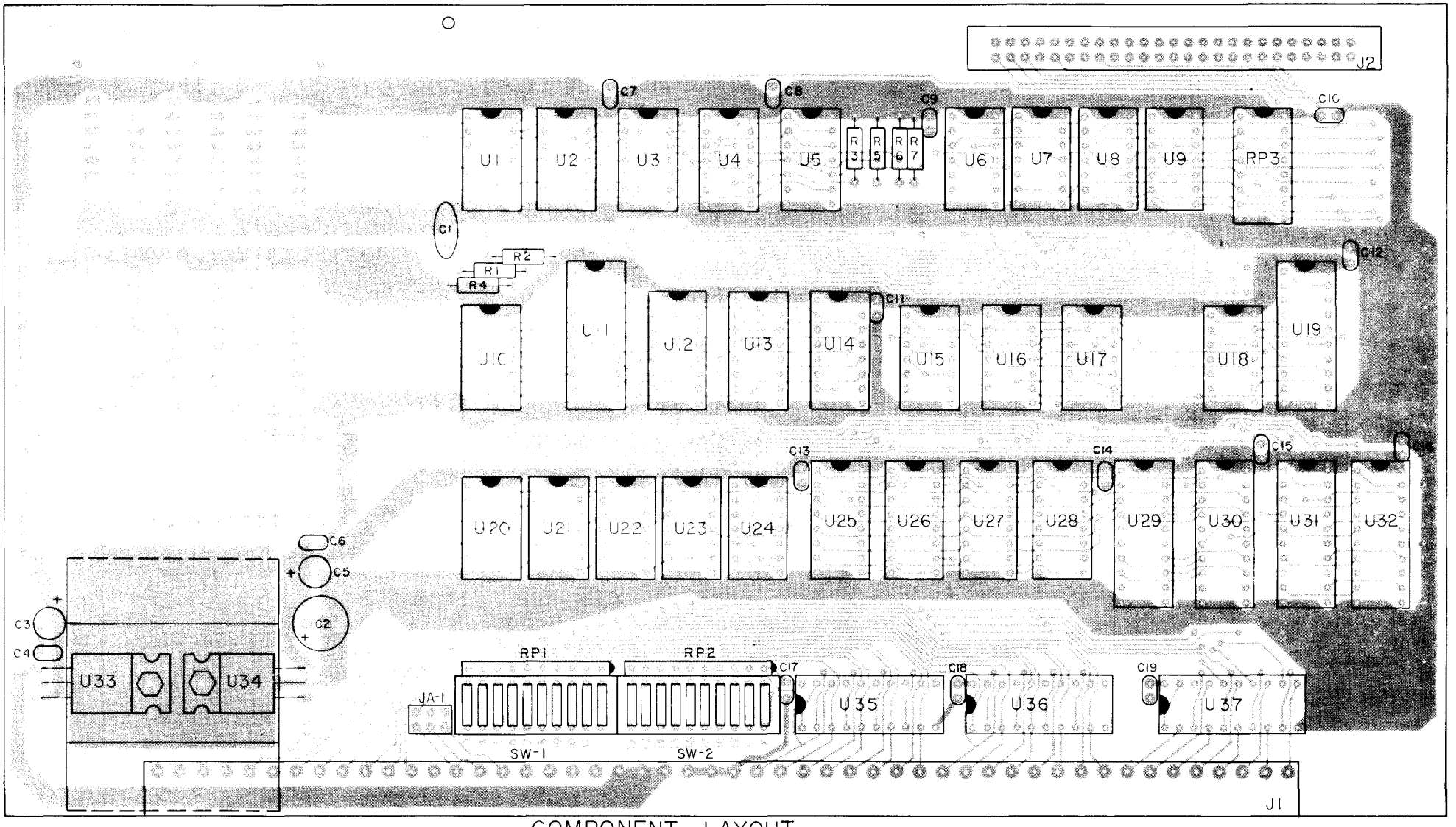

COMPONENT LAYOUT